ZLPLL User Guide

Wayne Knowles, ZL2BKC

[w.knowles@xtra.co.nz](mailto:w.knowles@xtra.co.nz)

<< Update Picture >>

Contents

[1 Introduction 3](#_Toc4361395)

[2 Specifications 3](#_Toc4361396)

[3 ZLPLL TCXO (ADF4351) Performance 5](#_Toc4361397)

[3.1 Phase Noise 5](#_Toc4361398)

[3.2 Output Level 5](#_Toc4361399)

[3.3 Harmonic Level 5](#_Toc4361400)

[3.4 Stability 6](#_Toc4361401)

[4 ZLPLL TCXO (ADF5355) Performance 6](#_Toc4361402)

[4.1 Phase Noise 6](#_Toc4361403)

[4.2 Output Level 6](#_Toc4361404)

[5 Application Notes 7](#_Toc4361405)

[5.1 Termination 7](#_Toc4361406)

[5.2 Power Supply 7](#_Toc4361407)

[5.3 Warm-up 7](#_Toc4361408)

[6 Features 7](#_Toc4361409)

[6.1 Frequency Multiplier Correction 7](#_Toc4361410)

[6.2 Channel Interface 7](#_Toc4361411)

[6.3 Programming 7](#_Toc4361412)

[6.4 Command Reference 9](#_Toc4361413)

[6.5 Frequency Calibration 10](#_Toc4361414)

[6.6 Diagnostics 10](#_Toc4361415)

[6.7 Status LED’s 10](#_Toc4361416)

[6.8 Initial Programming 11](#_Toc4361417)

[7 Special Applications 11](#_Toc4361418)

[7.1 TX Offset 11](#_Toc4361419)

[7.2 Sharing LO between 2 Tranverters 11](#_Toc4361420)

[8 Experimental Options 12](#_Toc4361421)

[8.1 2nd RF Output 12](#_Toc4361422)

[8.2 Low Frequency operation 12](#_Toc4361423)

[8.3 10MHz Filter Option 12](#_Toc4361424)

[8.4 Low Pass Filter 12](#_Toc4361425)

[8.5 Disable on-board oscillator power-down 13](#_Toc4361426)

[9 CW Beacon Firmware 13](#_Toc4361427)

[9.1 Configuration example 13](#_Toc4361428)

[9.2 Interfacing 13](#_Toc4361429)

[10 Application Notes 13](#_Toc4361430)

[10.1 23cm Transverter 13](#_Toc4361431)

# Introduction

The ZLPLL is a frequency agile synthesizer with many unique features designed for use as a local oscillator for amateur radio projects, weak signal source, or an exciter for a CW beacon.

Two versions of the board are currently available depending on frequency requirements with an onboard microprocessor catering for simple configuration of up to 16 frequencies that can be programmed by the end user over a serial interface.

As the programming and interfacing details are similar they are both included in this manual with specific differences between the boards highlighted where appropriate.

# Specifications

|  |  |  |
| --- | --- | --- |
| Model | ZLPLL TCXO | ZLPLL 14G |
| PLL | ADF4351 | ADF5355 |
| Frequency Range | 31MHz – 4.4GHz | 62MHz – 13.8GHz  (14 GHz with reduced specs) |
| Power | 8 to 14VDC  150mA | 9 to 14VDC  300mA |
| Onboard Reference | 26MHz TCXO | None |
| Stability | Typically +/- 100Hz at 1GHz  after 2 minute warmup | Governed by external reference |
| External Reference | +0dBm to +10dBm  Frequency: 10MHz (Default)  Custom frequency between 5 and 100MHz set in firmware | +0dBm to +10dBm  Frequency: 10MHz (Default)  Custom frequency between 5 and 200MHz set in firmware |
| Phase Noise | Typical Phase noise at 1GHz  -85dBc at 100Hz  -98dBc at 1kHz  -98dBc at 10kHz  -106dBc at 100kHz  -138dBc at 1MHz | Typical Phase noise at 10GHz |
| Outputs | 2 outputs at the programmed frequency, 180 degrees apart. | Output 1 = RF Out for 6.8 to 13.4 GHz  Output2 = RF Out for 62MHz to 6.8GHz |
| Output Level | 4 software selectable levels:  -3dBm/0dBm/+3dBm and +6dBm | Above 6.8GHz output:  Fixed +10dBm to +14dBm  Below 6.8GHz output:  +7dBm to 2GHz  0dBm at 5.7GHz |
| Provision for MMIC Amplifier | Yes (SOT-86) on output RF1 Only | No |
|  |  |  |
| CW Beacon Exciter Mode | Yes | Yes |
| Selectable Channels | 16 (Jumpers or BCD Interface) | 16 (Jumpers or BCD Interface) |
| Frequency Resolution | 1 KHz | 1 KHz  (1 Hz planned for a future firmware version) |

# ZLPLL TCXO (ADF4351) Performance

## Phase Noise

< Updated Picture >

Figure Performance

## Output Level

The Output level is dependent on the choice of inductor value in the output stage. The default 8.2nH inductors are suitable for frequency ranges above 1GHz and driving external multipliers.

For applications below 1GHz the inductor can be changed to 47nH which improves the output level for directly driving level 7 mixers up to 2GHz. This optional inductor is supplied with the board and can be fitted on request.

## Harmonic Level

The following graph can be used as a guide to determine the level of output for harmonics. As a general rule the lowest odd harmonic should be used to when wanting the highest level output on a given frequency.

## Stability

Because the ZLPLL uses an oven controlled xtal oscillator (OCXO) it has excellent frequency stability making this suitable for use on WSJT modes which require excellent stability over a 309 second to 1 minute period (depending on the mode being used).

With stability better than 1x10-10 the frequency error sufficiently allows for reliable frequency operation using all modes (including WSJT) up to 10GHz and potentially higher.

For more stringent frequency requirements an external oscillator such as Rubidium or GPSDO and the stability will be governed by the external reference.

# ZLPLL TCXO (ADF5355) Performance

## Phase Noise

Figure Performance

## Output Level

# Application Notes

## Termination

Ensure both outputs are well matched. If the 2nd output is un-used it should be terminated otherwise oscillations will occur especially at high output levels (L2 and L3).

## Power Supply

The on board voltage regulator is capable of operating up to 15V supply voltage. However for supply voltage above 9V the regulator will get very hot and it is advised to solder a small copper or brass strip to improve the heat dissipation.

## Warm-up

The recommended warm-up time is 5 minutes after applying power. For applications that demand short to medium term stability such as WSJT modes a warm-up period of 30 minutes is recommended.

When using an external reference no warm-up is required as stability is governed by the external reference.

# Features

## Frequency Multiplier Correction

In cases where the LO is followed by a frequency multiplier, in particular when multiplying by an odd number, the resulting frequency may suffer from rounding errors resulting in a small frequency error in the final frequency.

In order to prevent oddball frequencies (eg with 0.3333333 MHz re-occurring) the correct procedure is to set the ‘mult’ multiplier value to 3 and then program in desired frequency for the 3rd harmonic.

Due to limitations of the 8 bit Atmel processor only single precision math is supported in firmware various rounding errors occur after 76 significant digits. To overcome this restriction the “step” parameter can be set to force the rounding to the specified frequency step value. As this workaround is not completely failsafe final confirmation using a frequency counter is recommended if ultimate accuracy is required.

Example: Generate a Frequency of 10368.280 MHz for a beacon using the 3rd Harmonic

mult 3

step 10000

freq 10368.280

save 0

*Note: The frequency entered is the final frequency of the harmonic.*

## Channel Interface

## Programming

Programming can be done by connecting a **TTL** level RS232 interface onto the following pins of J4:

RXD, TXD, and GND

Baud rate: 9600 8 bits No Parity 1 stop bit

The interface levels are 3.3V but the protection circuits allow for 5V levels to also be connected without damage.

A suitable interface is a PL2303 based USB to RS232 converter, or a programming cable for a Yaesu FT8x7 transceiver.



The labeling of the pins on J4 assumes a DCE interface, thus the RXD pin is an input, and TXD is an output.

Use any terminal program, either TeraTerm, Putty or Hyperterm can be used.

uLO Universal Local Oscillator Rev3.1

(C)2012 W. Knowles, ZL2BKC

d

RF= 1152.000, L=3

Ref= 26.000, N= 0.025

ExtRef= 10.000

Params=23, CP=7

0 RF= 1152.000, L=3

1 RF= 1296.050, L=3

2 RF= 2400.050, L=3

3 RF= 3400.050, L=3

4 RF= 5760.050, L=3, M=3

5 RF=10368.050, L=3, M=3

6 RF= NAN, L=3, M=63

7 RF= 1242.000, L=3

8 RF= 4400.000, L=3

9 RF= NAN, L=3, M=63

10 RF= NAN, L=3, M=63

11 RF= NAN, L=3, M=63

12 RF= NAN, L=3, M=63

13 RF= NAN, L=3, M=63

14 RF= NAN, L=3, M=63

15 RF= NAN, L=3, M=63

The following example demonstrates the commands required to program channel 0 (the default if no channel switch installed) for 1920MHz:

M1

L3

F1920

S0

## Command Reference

Note: Commands are not case sensitive

| Command | Units | Description |
| --- | --- | --- |
|  |  |  |
| freq ##.# | MHz | Set the output frequency to the specified value in MHz.  Decimal numbers are permitted |
| level # |  | Set the output attenuator level.  0 = Minimum (typically -3dBm)  1 = typically 0dBm  2 = typically +3dBm  3 = Maximum (typically +6dBm)  Note for the >6.8GHz output on the ZLPLL14G board the level command is ignored and maximum output level is generated, typically > +10dBm |
| mode # |  | Set operating mode.  0 = RF Output disabled  1 = RF Output Enabled (LO Mode)  2 = CW Beacon mode. RF Output keyed with message  3 = CW Beacon mode. RF Output enabled with external keying |
| save # |  | Save current setup to memory channel # |
| channel # |  | Recall settings from memory channel # |
| ref\_int ## | MHz | Set frequency of internal reference. For ZLPLL this should be set to 26 MHz |
| ref\_ext ## | MHz | Set frequency of external reference in MHz. Default frequency is 10 MHz, but can be changed to any value between 5 and 100MHz |
| show |  | Display current configuration details |
| step # | Hz | Not supported |
| rdiv # |  | Reference frequency divisor. This should be set to 1 unless the loop filter components have been changed. |
| config mtld # |  | Mute to lock detect option. If the PLL is unlocked the RF Output will be disabled.  0=MTLD disabled  1=MTLD enabled |
| config spur # |  | Spur reduction mode  0 = Spur reduction disabled (lower Phase Noise)  1 = Spur reduction enabled (higher pahse noise) |
| config bleed # |  | ZLPLL 14G Only: Configure the loop filter bleed current.  Value is typically between 10 and 20 for best performance |
| config cp # |  | Phase Detector charge pump current. |
| config dblr\_max # |  | Frequency which the internal doubler is enabled on the reference input (either internal or external).  Refer to the PLL datasheet |
| config ref\_level # |  | Sensitivity level for external reference input. Default value = 10 |
| cw text |  | Enter the CW Message used for beacon mode transmissions (using mode=2 or mode=3) |
| cal |  | Enter TCXO Calibration routine. |
| adc |  | Diagnostic: Show levels of ADC input pins |
| diag |  | Diagnostic: Display PLL register values and frequency errors |

Note the frequency changes are volatile and must be saved using the save command if you require settings to be persistent.

## Frequency Calibration

## Diagnostics

The ADC command dumps the measured voltages of the

## Status LED’s

|  |  |  |  |
| --- | --- | --- | --- |
| LED | Name | Colour | Description |
| LED1 | Aux | Amber | Power Up  Permanently on to indicate self test failed  Standard LO Mode  Indicates the External Reference has been selected  CW Mode  Flashes to indicate the Key Down condition |
| LED2 | Lock | Green | Indicates the PLL is in a locked condition |

At power up the Lock LED will flash 3 times while running power up diagnostics. If the diagnostic passes the Green Lock LED will stay lit to indicate the PLL has passed self tests and is locked.

If any of the self tests fail the Amber Aux LED will stay permanently on and if the PLL has achieved Lock condition despite the fault the Green Lock LED will light.

For the TCXO version of the ZLPLL when an external reference is connected the Aux LED will flash for 3 seconds indicating the reference signal has been detected and stay lit to indicate the external reference has been detected. If a lock issue occurs using an external reference the firmware till revert back to the on board reference until it sees the reference removed and reapplied.

## Initial Programming

Several parameters have default settings, and if they are accidentally overwritten the performance of the board may be limited.

To reprogram the default settings, enter:

Ext\_ref 10

Int\_ref 26

Freq 1152

Level 3

Save 0

# Special Applications

The board is designed to cater for several end user applications. Some of the applications are outlined in this section.

## TX Offset

For some applications the LO frequency needs to be changed during transmit, for example generating a 20MHz repeater offset for a 1296 to 144MHz transverter.

When the TX line (shared with RS232 input) is pulled low the channel number is automatically increased by 8, or decreased by 8 for channels above 8.

## Sharing LO between 2 Tranverters

In order to reduce construction costs and maximize the use of space many constructors opt to share a single LO across multiple bands. Given the PLL board contains 2 LO outputs there is a natural instinct to use these for driving multiple transverters

If the LO frequency requirement is different for each transverter the TX input can be dropped to a logic LOW which results in 8 being added to the channel number, where the different LO frequency has been setup.

Note: The interface is 3.3V logic with a pull-up to logic 1. In most cases a suitable interface circuit may need to be added externally using a NPN transistor or similar.

# Experimental Options

## 2nd RF Output

The ADF4351 PLL chip provides 2 outputs with a phase difference of 180°. To enable the 2nd output remove R18 and install a 1206 0R jumper into location LPF2 and install the SMA connector.

Parts to add this option are supplied with the board.

## Low Frequency operation

The ADF4350 and ADF4351 datasheets recommend different output inductors depending on frequency range. If you require a few more dB of output on the lower frequencies then the inductors L4 and L5 can be changed as follows:

|  |  |
| --- | --- |
| Frequency Range | L4 and L5 Inductor Values |
| 137 to 500MHz | 100nH |
| 500 to 1000MHz | 47nH |
| 1000 to 2000MHz | 7.5nH |
| 2000 to 4400MHz | 3.9nH |

As supplied a 3.9nH inductor is installed suitable for > 2000 operation, and replacement inductors are supplied if more output power is required on lower frequencies.

Details of the expected power levels are shown in section 3.2

## 10MHz Filter Option

The external reference input at the PLL is a high impedance and extremely sensitive to external noise, or aliasing used on DDS reference. An optional 10MHz Xtal can be installed in location X1 if more filtering is required.

Note that the input resistor R10, 49.9Ω may be removed to increase level by 3dB .

## Low Pass Filter

When driving a frequency multiplier the LO harmonics generated are critical for producing a large signal after multiplication. However there are design applications where no multiplication is required and if there is insufficient filtering before the mixer this can result in unwanted images. For such applications a Minicircuits LFCN series Low Pass filter can be substituted with the 0Ω 1206 jumper installed in location LPF1 and LPF2.

## Disable on-board oscillator power-down

When an external reference is detected the internal oscillator is powered down for 2 reasons:

1. Power Reduction (saving approx. 50mA)
2. Reduce cross talk from internal oscillator which causes unwanted spurs

When the external oscillator is removed the internal reference starts from cold again and requires several minutes to warm-up, and 30 minutes to be become completely stable. By installing a 0Ω jumper in location R6 the internal reference is never powered off.

# CW Beacon Firmware

All boards feature the CW Beacon firmware by default. This is enabled by selecting mode 2 which is saved as part of the memory channel configuration.

When the message finishes it will loop back to the beginning with no delay, so inserting a space or delay is recommended.

The maximum message length is 100 characters

2 special characters are used to control the carrier as follows

|  |  |
| --- | --- |
| Character | Purpose |
| ^ | Send 1 second with carrier down |
| \_ (underscore) | Wait 1 second with no carrier |

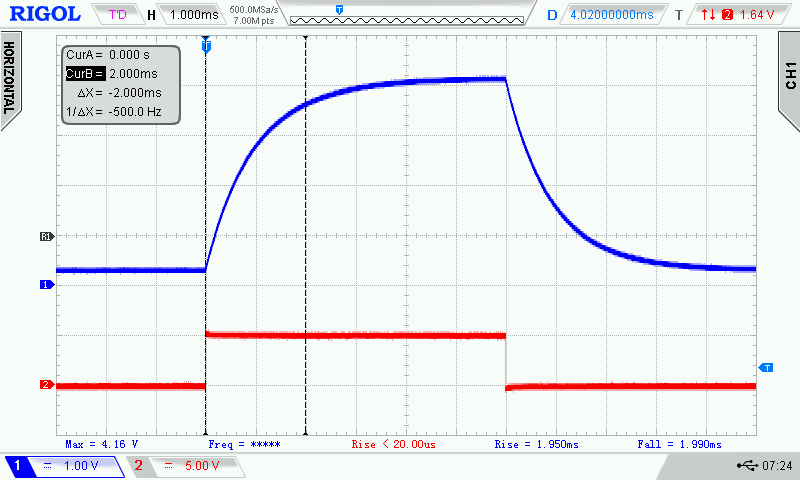
## Special Considerations

Due to the high frequency of the PLL chipsets the RF output has an extremely fast rise/fall time which ultimately results in a wide bandwidth “glitch” which amateur radio stations refer to as key clicks. On lower bands with higher channel densities and intermod potential it is desirable to implement envelope shaping to control key clocks. This cannot be done by the ZLPLL itself, however timing signals are available to interface to external PA’s to control the RF envelope.

The timing parameter t1 and t2 set the delay are as follows

<< Diagram of key timing >>

When interfacing to an external



## Configuration example

> cw text [ENTER]

\_ZLPLL\_EXAMPLE\_^^^^^ [ENTER]

>

# External Reference requirements

# Application Notes

## LO For 23cm Transverter

## LO for 76GHz transverter

## LO for 122GHz transverter

The narrowband segment of the 122GHz amateur band (2.5mm) starts at 122.250 GHz. One recommended lineup uses surplus 38GHz triplers (such as the CMA 38400 which operates at the required 40.7 GHz) and use the 3rd harmonic in the final mixer.

IF = 144MHz RF = 122250 MHz

Flo = 122106 MHz

FLO/3 (output of 38GHz module) = 40702 MHz

FLO/9 (input to 38GHz module) = 13567 1/3 MHz

In order to precisely configure this frequency the following setup is recommended:

freq 122106

multiplier 9

step 20000

save 0

For an IF of 145 MHz

freq 122105

multiplier 9

step 20000

save 0

## CW Beacon

# Troubleshooting

# FAQ

## Sometimes the frequency is displayed incorrectly

This is a side effect of the single precision math used in the on board micro. With careful use of the step parameter to round the frequency it is possible to control the output frequency however the displayed frequency as seen in the “show” output may be incorrect.

## Heat Issues

## Spurs

The onboard TXCO of the ZLPLL TCXO version is tuned using a PWM signal which can produce weak spurs about 50kHz each side of the programmed frequency. However they will disappear when using an external reference

Also you may see spurs at the harmonics of the reference frequency, especially if it falls within or near the loop bandwidth of the PLL.